REMARKS

In the Final Official Action mailed 20 April 2005, the Examiner reviewed claims 1-33. The Examiner rejected claims 1-33 under 35 U.S.C. §103(a).

Applicant has amended claims 1, 12, 23 and 29. Claims 1-33 remain pending.

The Examiner's rejection is respectfully traversed below.

Rejection of Claims 1-33 under 35 U.S.C. §103(a)

Claims 1-33 are rejected under 35 U.S.C. §103(a) as being unpatentable over Athanas *et al.* (US Patent No. 5,828,858) in view of Hillis *et al.* (US Patent No. 5,590,283).

Athanas *et al.* describes a "worm-hole run-time reconfiguration RTR" architecture, in which a data stream carries configuration information in a header file, for a set of functional units and a crossbar network interconnecting the set of functional units. The Examiner has taken the position that the network of Athanas *et al.* meets the limitation in the claims reading, "a plurality of routing units." Applicant submits that the Examiner's interpretation of the claim phrase is not supportable in the present application, for at least the reason that a crossbar network is a single routing unit (see claim 3, specification page 4, paragraph [0021]). Athanas *et al.* describes a system in which a single crossbar network is configured for routing streams of data among a set of functional units, and therefore does not teach the limitation recited in the claim.

Although it is not clear to Applicant how the Examiner reads the claim limitation "a plurality of routing units" on a single crossbar network, Applicant has amended the independent claims 1, 12, 23 and 29, without loss of scope, to clarify that routing units in the plurality of routing units of the claim are coupled to respective subsets of functional units. The crossbar network of Athanas *et al.* is coupled to all the functional units, and there is no other routing unit described in Athanas *et al.*

This amendment emphasizes a feature of the present invention (present in the original claims, as interpreted by Applicant) that multiple routing units are configured in parallel within a function cycle, and that such routing units are coupled to different sets of functional units. No reference suggests this structure.

In addition, Applicant submits that Athanas et al. does not describe the "control word distribution circuitry" recited in claim 1, and in the other independent claims. The Examiner refers to Fig. 2, element 21 as satisfying the limitation "control word distribution circuitry." The cited description in Athanas et al. shows a logical organization for a header of a data stream,

which includes the source and destination identifiers. There is no discussion whatsoever in Athanas et al. of circuitry used to distribute the control words in that header among routing units. Rather, Athanas et al. suggests, without describing explicitly, that the header of the data stream is delivered serially through the data port, through which the data of the data stream is delivered. The serial delivery of the individual words in the header via the data port is substantially different than the "control word distribution circuitry which supplies a routing control signals in parallel..." as recited in claim 1, and in the other independent claims.

The Examiner relies upon the concept of "synchronous processing" as described in Hillis et al. to suggest that the functional units of Athanas et al. could be modified to deliver output data within a function cycle, and that the control word distribution circuitry would supply routing control signals in parallel for the function cycle.

As described above, Athanas et al. describes a system in which control words from the header of a data stream are supplied serially, rather than in parallel. The concept in general of synchronous processing does not suggest that a plurality of routing control units, as claimed, should be configured synchronously, and in parallel, for routing data among a plurality of functional units.

Hillis et al. describes a massively parallel computing system with a data routing architecture base on message passing among routing nodes. (See, Figs. 2A, 2B and 3, and column 6, line 53 to column 12, line 5.) The data routing architecture of Hillis et al. is not similar to the data routing architecture claimed herein.

Therefore, the combination relied upon by the Examiner does not include at least the limitations recited in claim 1 of "a plurality of routing units...", and of "control word distribution circuitry..." which operates in parallel. Because the combination does not include all of the elements of claim 1, the prima facie case of unpatentability is incomplete. Likewise, the prima facie case of unpatentability is incomplete as to each of the other independent claims 12, 23 and 29 for at least the same reasons.

In connection with claim 2, the Examiner takes the position that the elements 32 and 34 of Fig. 3 meet the limitation of a "multiplexer..." The element 32 is the crossbar network discussed above, which constitutes a single routing unit. The element 34 is a multiplier. It is unclear how the Examiner equates the crossbar network of Athanas et al. with the claimed multiplexer, when the same element is relied upon as suggesting a crossbar with respect to claim 3. Clarification is respectfully requested.

In connection with claim 5, the Examiner takes the position that the processing elements PE 11(0) to 11(N) of Hillis *et al.* correspond with logic blocks as recited in claim 5, with the comment "noting interfaces to control network and data router". The Examiner is apparently equating the control signals applied to the control network, and the routing signals supplied to the data router to the "output from one of the plurality of available functions..." The claim requires however that the functional unit include logic to select one of the outputs. There is no similar structure described in Hillis et al. Indeed, there is no description of the structure of the processing elements provided at all in Hillis et al. Therefore, the Examiner is believed to be misreading the reference.

In connection with claim 6, the Examiner takes the position that the data ports of Athanas et al. constitute memory within a functional unit, and relies on the header structure described in Fig. 2 to suggest the control word distribution circuitry. As discussed above in connection with claim 1, the header is delivered serially through the data ports. There is no discussion concerning how the read and write control words on the data ports are associated with such headers, or with any other routing control words in Athanas et al. Furthermore, there is no control word distribution circuitry described by the reference. Therefore, the Examiner is believed to be misreading the reference.

In connection with the claim 7, the Examiner relies on Hillis et al. the data router element 15 of Fig. 1, and argues that it would be "a matter of obvious design choice as to what hardware component provides what information." As discussed above, the data router in Hillis et al. operates on a message passing architecture. There is no suggestion whatsoever concerning the delivery of addresses to memory within functional units using that message passing structure, and more importantly, no suggestion concerning the delivery of such addresses in parallel distribution circuity as required by the claim. Therefore, the Examiner is believed to be misreading the reference.

In connection with claim 8, the Examiner relies on the same combination of elements as relied upon in connection with claim 7, along with the vague comment that it would be "a matter of obvious design choice as to what hardware component provides what information." Claim 8 differs from that claim 7, in that the addresses are supplied by the functional units, rather than via the control word routing circuitry. However, Applicant submits that the structure of Hillis et al. does not contemplating one functional unit, such as a processing element PE 11, supplying

address for memory in a functional unit in the configuration recited in claim 8. Therefore, the Examiner is believed to be misreading the reference.

In connection with claim 9, the Examiner cites column 6, lines 12-16 of Athanas et al. The cited passage mentions a "loop mode" operation of the worm-hole RTR system. According to the loop mode, only one operand is processed at a time. It is unclear however how this relates to a functional unit being dedicated logic as required in claim 9. The functional units of Athanas et al. include a plurality of generic units, along with a special-purpose multiplier, that may be dedicated logic. The functional units however are not interconnected is required by the claims herein.

In connection with claim 10, the Examiner cites column 5, lines 57-64 of Athanas et al. The cited passage mentions a "view" of the architecture which includes a "relatively static pipeline." It is unclear how this citation relates to hardwired special-purpose logic for use as a functional unit as required by claim 10. Nonetheless, the functional units in the references are not interconnected as required by the claims herein via a plurality of routing units.

In connection with claim 11, which requires synchronous operation, the Examiner relies on the combination of Athanas et al. and Hillis et al. as discussed above in connection with claim 1. Claim 11 is believed patentable for at least the same reasons as claim 1.

In connection with claim 12, the Examiner takes the position that the architecture of Athanas et al. could be applied according to the architecture of Hillis et al., and that the result would lead to the limitations of claim 12. Claim 12 describes a system in which processing blocks having an architecture like that of claim 1, are arranged with block level routing units and routing control signal distribution circuitry. It is submitted for the reasons discussed above, that the references do not suggest architecture of claim 1, and therefore claim 12 which incorporates the architecture recited in claim 1 within a processing block, is patentable for least the same reasons.

Furthermore, the Examiner reads processing block level features of claim 12 on Hillis et al. Applicant submits that the Examiner is misreading the reference. In particular, the Examiner reads the "plurality of routing units" on the control network 14 of Hillis et al., and reads the "block level control word distribution circuitry..." on the control network 14 and the data router 15 of Hillis et al. The control network 14 of Hillis et al. does not steer data and therefore does not constitute a plurality of data routing units. Thus, it is submitted that the Examiner is misreading the reference.

In addition, there is no discussion in Hillis et al. that suggests that the combination of the control network 14 and data router 15 operate to deliver control words for function cycles, to the any data routing unit, as required by the claimed block level control word distribution circuitry. Thus, it is submitted that the Examiner is misreading the reference.

Finally, the combination suggested by the Examiner would involve using the worm-hole RTR system of Athanas et al. as a processing element in Hillis et al. Claim 12 does not read on such a combination, as explained above. Furthermore, the Examiner suggests that the motivation to do so arises from the teaching of Hillis et al. as it relates to data flow among a large number of processors. Applicant submits that there is no reason in the record to suggest that the worm-hole RTR architecture is reasonably likely to be a successful choice in the massively parallel system of Hillis et al. Therefore, the prima facie case for unpatentability is incomplete because not all elements of the claims are found in the reference, and because there is no motiviation to combine the references to achieve the claimed invention.

As to claims 13-21, the Examiner suggests that they are unpatentable for the reasons discussed with reference to claims 2-10. Applicant respectfully submits that claims 2-10 are patentable as described above, and that therefore claims 13-21 are patentable. Furthermore, the combinations reciting claims 13-21 arising in the hierarchical architecture of claim 12 are separately patentable, at least for the same reasons as claim 12.

In connection with claim 22, the Examiner relies on Hillis et al. to suggest synchronous operation of control word distribution circuitry. As discussed above, none of the references describes control word distribution circuitry that delivers control words to a plurality of routing units in parallel, as set forth in the claims. Furthermore, the general concept of synchronous processing mentioned in the passage of Hillis et al. cited by the Examiner does not suggest synchronous operation of control word distribution circuitry for a plurality of routing units and a plurality of block level routing units as claimed. Accordingly, it is submitted that the Examiner is misreading the references.

In connection with claims 23, the Examiner relies upon Hillis et al. to suggest the limitation of providing a plurality of software routing control signals in parallel to a plurality of routing units, citing the control network 15 of Hillis et al. The control network of Hillis et al. is arranged in a tree configuration, and operates according to a message passing architecture. See, column 13, lines 19-39. The message packets are not supplied in parallel to a plurality of

functional units in the Hillis et al. architecture. Accordingly, it is submitted that the Examiner is misreading the reference.

In connection with claim 28, the Examiner relies on the general concept of synchronous processing mentioned in Hillis et al. As argued above, the general concept of synchronous processing mentioned in the passage of Hillis et al. cited by the Examiner does not suggest synchronous operation of control word distribution circuitry for a plurality of routing units.

In connection with claim 29, the Examiner basically relies on the same combination of Athanas et al. and Hillis et al. as applied to claim 12. Applicant submits that the method recited in claim 28 is patentable for the reasons discussed above in connection with claims 12 and 23.

The Examiner takes the position that claims 30-31 are unpatentable for the reasons discussed in connection with claims 9-10. Applicant requests reconsideration for the reasons discussed above.

The Examiner takes the position that claims 32-33 are unpatentable for the reasons discussed in connection with claims 27 and 24. Applicant requests reconsideration for the reasons discussed above.

Accordingly, reconsideration of the rejection of claims 1-33 as amended is respectfully requested.

CONCLUSION

It is respectfully submitted that this application is now in condition for allowance.

The Commissioner is hereby authorized to charge any fee determined to be due in connection with this communication, or credit any overpayment, to our Deposit Account No. 50-0869 (UNMI 1000-1).

Respectfully submitted,

Dated: 29 July 2005

Mark A. Haynes, Reg. No. 30,846

HAYNES BEFFEL & WOLFELD LLP
P.O. Box 366
Half Moon Bay, CA 94019
(650) 712-0340 phone
(650) 712-0263 fax